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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Ehood Geva

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LAW OFFICE OF IDO TUCHMAN (SJO)

69-60 108TH STREET

SUITE 503

FOREST HILLS, NY 11375

EXAMINER

NGUYEN, HOA CAO

ART UNIT

PAPER NUMBER

2841

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/690,113	<b>Applicant(s)</b> GEVA ET AL.	
	<b>Examiner</b> Hoa C. Nguyen	<b>Art Unit</b> 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 December 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 and 17-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 17-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date: _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>1 page</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

1. Applicant's election without traverse of group I, claims 1-9 and 17-23, in the reply filed on 15 December 2005 is acknowledged. Claims 10-16 and 24-26 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention group, there being no allowable generic or linking claim. Claims 1-9 and 17-23 are considered in this Office Action.

#### ***Specification***

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Shielding Structure For Conductive Traces on a Circuit Board.

#### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. See MPEP § 2173.05(c). Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat.

Art Unit: 2841

App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 3 recites the broad recitation **the conductive trace**, and the claim also recites **the signal trace** which is the narrower statement of the range/limitation.

For the purpose of this Office Action, examiner assumes the conductive trace and the signal trace is the same structure, the structure of a transmission/data line (a conductive line).

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-9 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimada et al. (US 6353189).

**Regarding claim 1**, as shown in figure 1, Shimada et al. disclose a trace cover suitable for shielding a conductive trace 1 (a transmission line - signal trace) on a circuit board, the circuit board includes at least one circuit ground, the trace cover comprising:

(a) A body 3 (insulating layer) composed of a dielectric substrate (insulating material), see column 21, lines 9,

(b) the body having a top surface (facing layer 4), a bottom surface (facing layer 5) and side surfaces (facing conductive pillars 7a),

(c) the bottom surface of the body configured to be disposed substantially over the conductive trace 1 (transmission line - signal trace), see column 4, lines 49-58; and

(d) top shielding 4 (a conductive layer) disposed on the top surface of the body,

(e) the top shielding being electrically coupled with the at least one circuit ground of the circuit board (ground voltage), see column 21, lines 29-30.

**Regarding claim 2**, as shown in figure 1, Shimada et al. further disclose:

(a) side shielding 7a (conductive pillars) perpendicular to the direction of the signal trace 1,

(b) and substantially parallel to the length of the conductive trace (with conductive layers 4 and 6, the side shielding 7a covered along transmission line 1, 360° around the transmission line 1), see column 21, lines 26-33, and column 4, lines 22-27, and

(c) the side shielding being electrically coupled with the at least one circuit ground of the circuit board (grounding through shield pattern 2, a via land or a pad), see column 21, lines 28-33.

**Regarding claim 3**, as shown in figure 1, Shimada et al. further disclose at least one connecting pad 2 (shield pattern - via land) disposed on the bottom surface of the

body, the connecting pad configured to electrically couple the side shielding with the at least one circuit ground, see column 4, lines 49-58.

**Regarding claim 4**, as shown in figure 1, Shimada et al. disclose the side shielding 7a includes a plurality of conductive vias (conductive pillars) disposed between the top surface and bottom surface of the body, see column 4, lines 17-18.

**Regarding claim 5**, Shimada et al. disclose the plurality of conductive vias are spaced themselves with a prescribed distance apart, see column 17, lines 45-48. The prescribed distance apart is inherently including the approximately one-quarter inch apart.

**Regarding claim 6**, as shown in figure 10, Shimada et al. disclose the side shielding includes a conductive plating 35B (conductor layer 35B) disposed along the side surfaces of the body, see column 24, lines 27-35.

**Regarding claim 7**, as shown in figure 10, Shimada et al. disclose the top shielding is a conductive plating (electroless plating), see column 24, lines 34-45.

**Regarding claim 8**, Shimada et al. disclose every limitation as shown in claim 2 above.

**Regarding claim 9**, the dielectric substrate of the body is different than a dielectric substrate of the circuit board, see column 6, lines 50-55.

**Regarding claim 17**, as shown in figures 1 and 10, Shimada et al. disclose every limitation as shown in claim 1-9 above.

7. Claims 18-20 and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Johns (US 4816616).

**Regarding claim 18**, as shown in figures 1F and 2, Johns discloses a trace cover suitable for suppressing electromagnetic emissions from a conductive bus on a circuit board (see column 1, lines 20-23), the conductive bus including at least two substantially parallel bus traces 30, the circuit board including at least one circuit ground G (see column 2, lines 7-10), the trace cover comprising:

- (a) A body 40 (second dielectric layer) composed of a dielectric substrate,
- (b) the body having a top surface (facing conductive layer 50), a bottom surface (facing the conductor traces 30 and layer 20) and side surfaces (facing conductive layer 50),
- (c) the bottom surface of the body configured to be disposed substantially over the conductive bus 30, as shown in the figure 1F;
- (d) as shown in figure 1F, side shielding (the section of conductive layer 50 formed along the side surfaces of the body) perpendicular to the direction of the conductive bus and substantially parallel to the length of the conductive bus (the layer 50 formed along the conductor traces 30),
- (e) the side shielding being electrically coupled with the at least one circuit ground of the circuit board, see figure 2 and column 2, lines 7-10;
- (f) and top shielding (the section of upper conductive reference layer 50 formed on top of layer 40) disposed on the top surface of the body, see column 3, lines 38-40.

(g) the top shielding being electrically coupled with the at least one circuit ground of the circuit board, as shown in figure 2.

**Regarding claim 19**, as shown in figures 1F and 2, Johns further discloses bus shielding (the section of conductive layer 50 in between the conductor 30) disposed within the body and between the bus traces 30 (the conductors), and as shown in figure 2, the bus shielding being electrically coupled with the at least one circuit ground G of the circuit board.

**Regarding claim 20**, as shown in figure 2, Johns further discloses at least one connecting pad 10 (the conductive reference layer 10 is considered as a connecting pad for grounding and for encircling the bus traces 30) disposed on the bottom surface of the body, the connecting pad configured to coupled the bus shielding with the at least one circuit ground. It is noticed that, in figure 2, the body comprises dielectric cap 25 and dielectric sidewall 45, see column 3, lines 65-68.

**Regarding claim 22**, as shown in figure 2, Johns discloses the bus shielding (the conductive layer 50) is coupled to the circuit ground through the side shielding.

**Regarding claim 23**, Johns discloses the side shielding includes a conductive plating disposed along side surfaces of the body, see column 3, lines 38-40. It is noticed that the depositing conductive layers inherently includes both electroplating and electroless plating.

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:



Art Unit: 2841

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johns and further in view of Shimada et al.

Johns discloses every limitation as shown in claim 19 above, but failed to disclose the bus shielding includes a plurality of conductive vias disposed between the top surface and bottom surface of the body.

As shown in claims 1-9 above, Shimada et al. disclose one of the shielding structures for suppressing electromagnetic emissions (see column 1, lines 6-9) containing conductive vias 7a (conductive pillars) surrounding along the sides of the transmission line 1. It is noted that Shimada et al. also disclose every limitation in claims 18-23 except the at least two substantially parallel bus traces.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from Shimada et al. to form a plurality of conductive vias disposed between the top surface and bottom surface of the body 40 of Johns' teachings instead of depositing conductive layer 50 in between the conductors 30 for packaging of high density circuit board with high productivity. It is noticed that in applying the teachings from Shimada et al., the depositing conductive layer 50 in between the conductors 30 is no longer necessary and the layer 50 can be easily formed by applying a sheet of metal over the top of the body 40.

***Citation of Relevant Art***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kwong (US 6444922) discloses a zero cross-talk signal line design.

Kwong et al. (US 6608258) disclose a high data rate coaxial interconnect technology between printed wiring boards.

Kwong et al. (US 6872595) disclose a technique for electrically interconnecting signals between circuit boards.

Ozeki et al. (US 20020060090) disclose a printed circuit board and manufacturing method of the printed circuit board.

Matsubayashi et al. (US 5426399) disclose a film carrier signal transmission line having separating grooves.

Kawakami et al. (US 4885431) disclose a printed circuit board.

Selk et al. (US 5677515) disclose a shielded multilayer printed wiring board, high frequency, high isolation.


### ***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen  
4 January 2006



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